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Design of Monotonic Digitally Controlled Oscillator (DCO) for Wide Tuning Range

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***Abstract*— An analytical equation to make a trade off between tuning range and differential non-linearity (DNL) for a digitally controlled oscillator (DCO) is derived and based on the equation, an optimization method to obtain monotonic behavior of DCO is proposed. To verify the approach, a 12 bit DCO is designed, in 0.18 μm CMOS technology. The designed DCO has achieved Differential Non-linearity of -0.41 LSB without degrading other parameters. The DNL achieved is within the limit and designed DCO shows highly monotonic behavior over the entire tuning range from 3.12 GHz to 4.15 GHz (30% of the tuning range). The simulated phase noise is –135.2 dBc/Hz (@ 4 MHz offset) at oscillation frequency of 3.6 GHz with 14.2 mW power consumption.**

***Index Terms*—Digitally Controlled Oscillator, Monotonic, Wide tuning range, Phase noise, 0.18 μm CMOS.**

I. Introduction

Recent trend of implementing digitally controlled RF circuits in deep submicron CMOS technology is very attractive, due to its improved frequency characteristics and high integral ability. Furthermore, limited voltage headroom that provides very steep and compressed linear range for analog circuits design favors the digital assisted approaches in analog circuits [1]. Digitally controlled oscillators [DCO] [2]-[6] whose output frequency is a function of digital controlled word (DCW), is also an example of analog circuit implemented using digital assisted approaches.

In LC-DCOs, DCW changes t(e capacitance of varactor cel, "y switching between high and low level voltages to tune oscillation frequency. The varactor cell is implemented in capacitor array. This capacitor array is implemented in blocks such as block for compensation for process, voltage, and temperature (PVT) variations, coarse tuning block (CTB), fine tuning block (FTB), tracking bank etc for tuning.

DCO same as voltage controlled oscillator (VCO) are designed for different wireless standards same which have many strict requirements such as phase noise, wide tuning range, linearity and so on. Besides these DCO has other Parameters characteristic like step size, monotonic behavior to be full fill. These Digital characteristics are important during locking of all-digital phase locked loop (ADPLL) used as local oscillator (LO) in wireless transceiver. In locking process, ADPLL first captures and then locks with the RF frequency, so the output frequency must be linear and monotonic for

Smooth locking with the DCW generated by the digital phase frequency detector. This is very important parameters of the DCO which has not been given much attention in DCO design reported so far [2]-[6].

DCO [2] is implemented in ring topology which has poor phase noise and high power consumption with low operating frequency so it is not suitable for high frequency wireless communication applications. DCOs [3]-[6], implemented in LC topology have capabilities to operate at GHz with good phase noise performance but have narrow tuning range. Therefore, variable capacitor bank is used to obtain higher tuning range in the design of a DCO.

To achieve fine tuning frequency step, capacitor array is implemented using multiple blocks [3][5] and simultaneous switching is not allowed. This may improve the linearity but used many digital inputs which increase varactor area and interconnect parasitic capacitance.

Most of the above mentioned DCOs were concerned about frequency tuning steps and less concerned about linearity. No analytical approaches have been reported so far to trade-off between DNL, tuning range and mismatch in capacitive array for optimization of the DCO design which can provide a systematic approach in the selection between the number of varactor arrays and coding scheme i.e. binary weighted coding, thermometer coding or segmented coding to implement the varactor cells in the array.

In this paper we have analyzed nonlinearity of a DCO using nonlinear mathematical equations, mismatch among the tuning elements and systematic and graded errors and derived an analytical equation which provides a systematic approach to design monotonic DCO for large tuning range and limited permissible DNL. Based on the above model, 12 bits DCO

was designed in 0.18 µm CMOS technology to check the mathematical concept.

2. Non-linearity Consideration in DCO Design

2.1 Basics

In a conventional cross-coupled LC-oscillator [7][8] the oscillating frequency is decided by the parallel resonance of LC tank. Frequency tuning can be achieved by either varying the inductance (L) or the capacitance(C). However, capacitor is varied to achieve fine tuning step, wide tuning range and less chip area.

In Fig.1. equivalent circuit of a functional LC-DCO is shown. The DCO consists of an inductor L, varactor array implemented by a parallel combination N varactor cell and a negative resistance (-R) MOS pair. The negative resistance is used to compensate the losses of the capacitor and the inductor and implemented by cross-coupled MOS pair.

The oscillating frequency (*f*) of binary weighted N-bit DCO is given by Equation (1)

$$f = \frac{1}{2\pi\sqrt{L\cdot(C_P + \sum_{k=0}^{N-1} C_k)}} \quad (1)$$

where, $C_k = 2^k \cdot (C_0 + \overline{d_k} \cdot \Delta C_{LSB})$ (2)

Where N is the number of control bits, C_P is the parasitic capacitance which includes the capacitance of inductance, cross-coupled transistors capacitance, drivers capacitance and all interconnection capacitance etc., *L* is the total inductance. In Eqn. (2) capacitor (C_k) consists of low state and high state capacitance of K^{th} bit. d_k represents digital status of K^{th} digital control bit and ΔC_{LSB} is the effective switchable capacitance of LSB and decides tuning step. Digital control bits (d_k) are inverted to represent high capacitance value for low digital state and vice versa. This locks oscillation frequency with digital codes.

2.2 Non-Linearity and Tuning Range

In a conventional VCO, gain is measured by *Kvco* = (*ΔF*)/(*ΔV*) where *ΔF* is the change in frequency due to the change in the control voltage (*ΔV*). If the transfer curve is straight, that shows the high linearity and for monotonic function the slope of the line should not be negative even when (*ΔV*) tends to zero. But in case of DCO, the transfer characteristic is not continuous rather it is discrete. Therefore gain is the change in oscillating frequency for LSB switching. So linearity for DCO is expressed in terms of DNL. If the ratio of maximum step (ΔF_{max}) and minimum step (ΔF_{min}) to average step (ΔF_{Ideal}) is less than 1.5 and greater than 0.5 respectively, the DCO is assumed to be linear and monotonic. The minimum step size of DCO with switching of LSB is calculated using Equation (1). Since the switching capacitance of LSB (ΔC_{LSB}) is very small as compared to the total capacitance, the step size can be easily approximated Taylor's equation in Equation (1) and is given in Equation (3).

$$\Delta F \cong 2\pi^2 \cdot F^3 \cdot L \cdot (\Delta C_{LSB}) \quad (3)$$

Where *ΔF, F* and *L* are frequency step size, center frequency and inductance, respectively. Equation (3) has not included the effects due to mismatch variation among the varactor cells. Frequency step size is calculated for n^{th} code (ΔF_n) with mismatch variation in Equation (4).

$$\Delta F_n \cong 2\pi^2 (F_{n-1} + \Delta F_{n-1})^3 \cdot L \cdot \Delta C_{LSB} (1 + T_s \cdot \sigma(\Delta C)) \quad (4)$$

Here, F_{n-1} *and* ΔF_{n-1} are oscillating frequency and frequency step for $(n-1)^{th}$ digital control code. σ(ΔC) represents standard deviation for variation in switching capacitance. T_s is a constant which decides permissible variation for required yield. Equation (4) shows that the frequency step depends on center frequency and mismatch for equal switching capacitance.

Consider a DCO with tuning frequency from F_1 to F_2. The minimum and maximum step size can be obtained on the lowest frequency (F_1) and highest frequency (F2) when switching capacitance have minimum and maximum value due to maximum variation and given by Equations (5) and (6), respectively. Ideal step is derived by replacing *F* from Equation (7) to Equation (3).

$$\Delta F_{min} \cong 2\pi^2 \cdot F_1^{\,3} \cdot L \cdot (\Delta C_{LSB} (1 - T_s \cdot \sigma(\Delta C))) \quad (5)$$

$$\Delta F_{max} \cong 2\pi^2 \cdot F_2^{\,3} \cdot L \cdot (\Delta C_{LSB} (1 + T_s \cdot \sigma(\Delta C))) \quad (6)$$

$$F = \sqrt{F_1 F_2} \quad (7)$$

So for DNL ≤ 0.5 LSB, maximum step size and minimum step size ratio with ideal step size should be less than 1.5 and greater than 0.5, respectively. This is given by Equations (8) and (9). Equation (10) defines the tuning range (TR %) in terms of minimum (F1) and maximum (F2) frequency.

$$\frac{\Delta F_{max}}{\Delta F_{Ideal}} = \left(\frac{F_2}{F_1}\right)^{\frac{3}{2}} \cdot (1 + T_s \cdot \sigma(\Delta C)) \le 1.5 \quad (8)$$

$$\frac{\Delta F_{min}}{\Delta F_{Ideal}} = \left(\frac{F_1}{F_2}\right)^{\frac{3}{2}} \cdot (1 - T_s \cdot \sigma(\Delta C)) \ge 0.5 \quad (9)$$

$$TR\,(\%) = \left(\frac{F_2 - F_1}{F}\right) \times 100 \quad (10)$$

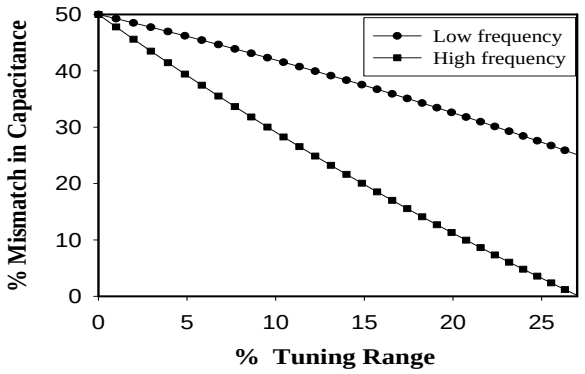


Fig.1. Optimization curve between tuning range and mismatch capacitance for DNL=0.5 LSB.

To take the effect of nonlinear mathematical equation on frequency step, a graph, shown in Fig.2. is plotted using Equations (8), (9) and (10) between TR (%) and permissible capacitance mismatch (%).This graph can be used for any center frequency. For example if tuning range is 10%, then permissible variation in capacitance is 28% whatever be the center frequency. The two lines in Fig.2 show the permissible variation in capacitance for minimum frequency and maximum frequency. Since the frequency step at higher frequency is always greater than lower frequency, the permissible capacitance mismatch will also be higher. So, only higher frequency curve is sufficient to calculate variation in capacitance.

3. Design of 12 bit DCO

3.1 DCO Core

The proposed structure of LC-DCO is shown in Fig.3. The center tap on chip inductor (L) in parallel with capacitor bank makes parallel resonance. Two cross-coupled NMOS transistor M1 and M2 provide the necessary gain to compensate loss in the resonator and to sustain oscillations. 12 bit Capacitor bank is used for required tuning range. This is implemented by two parts. First part has 2-bit MIM capacitor in series with NMOS transistors for coarse tuning. Second, is implemented by PMOS pair for fine tuning step.

DCO is designed to reduce the performance degradation and to achieve good DNL. The center tap differential inductance provided by 0.18 μm TSMC 1P6M CMOS process with 3 turns is used to get high quality factor (Q-factor) with symmetrical structure and better coupling coefficient [9]. High Q-factor inductance reduces LC tank loss and improves phase noise performance. Also, the Q-factor of capacitor is improved by reducing the parasitic.

Simulation is performed to trade off between phase noise and tuning range. The maximum tuning range without degrading the phase noise is approximately 30% at 3.6 GHz center frequency. This is the coarse tuning range (CTR). Fig.2 shows that if the tuning range is more than 26% then the permissible variation in mismatch among the varactor cell is zero which is practically impossible to achieve. So, this CTR is divided in four parts implemented with 2-bits which has 10% tuning range for one part with 28% permissible variation in capacitance. This CTR is large and is achieved by the large switching capacitance devices. Metal insulator metal (MIM) capacitors in series with NMOS transistor implemented in binary weighted coding are suitable candidate.

The important parameter here is that the switching capacitance of FTB should be greater than switching capacitance of CTB for its any digital code.

Please note that in this design we fixed the smallest frequency tuning step to be 0.4 MHz to prove the proposed optimization method. So, if the frequency tuning step is 0.4 MHz, the number of required digital bits for given FTR is decided by step size. Therefore, for FTR of 300 MHz, 10 bits are sufficient when frequency step is 0.4 MHz.

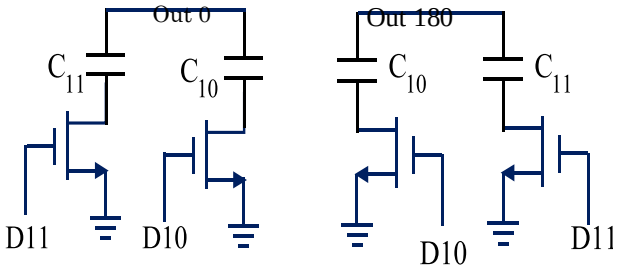


Fig.2. Detail of MIM capacitors implementation in proposed DCO.

This 10 bits varactor array is implemented with segmented architecture. PMOS transistors are used as varactors. Varactor size is decided for 0.4 MHz frequency step at the central frequency of 3.6 GHz. This is optimized for large tuning range, by selecting the higher value of C_{max} /C_{min} with minimum area. The dimension of PMOS for the varactor is W=220 nm and L=500 nm for LSB. Monte-Carlo simulation is performed to calculate the mismatch variation for the identical cells. Standard deviation value is 1.46% of the nominal value. For a 99.5% yield, the value of T_s is 2.871. So, permissible variation in capacitance for LSB is 4.2%. The permissible capacitance variation is equally divided between graded errors and mismatch. So, mismatch is limited to be 14%. The number of binary bits and thermometers bits for required DNL is determined to be 2 and 8, respectively [9].

The 8 bit thermometer decoded cells are implemented in 16 by 16 matrixes. 2-bit binary weighted cells are placed at the center of matrix. Identical varactor cell are made by connecting 4 PMOS pair in parallel for binary weighted and thermometer decoded varactor cell to improve matching in FTB. One and two pairs of PMOS are electrically connected for lower order binary bits.

3.2 Digital Circuits

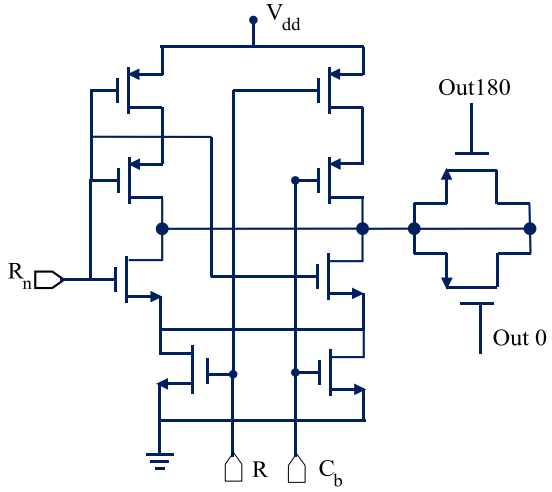
10 bit FTB is implemented with 8 bit thermometer decoding and 2 bit binary weighted varactor cell. The digital circuits are used to implement proposed logic decoder. This decoder decreases the area of varactor array and parasitic at schematic as well as at layout level. The row, column and local decoder are implemented with minimum size logic gates.

The decoding scheme is demonstrated here for 4 bits. 2 bits (D3-D2) are row bits and 2 bits (D1-D0) are column bits. In the proposed scheme, the row decoder and column decoder take binary weighted input signal and generates the signal as shown in table I(A) & I(B). Then, these lines (R1-R4 and C1-C4) are routed in the varactor array and fed to local decoder adjacent to varactor cell. Local decoder generates appropriates signal to varactor cell. The local decoder schematics for even and odd rows are shown in Fig.5.

TABLE I (A): TRUTH TABLE OF ROW DECODER

INPUT signal		OUTPUT signal			
D3	D2	R1	R2	R3	R4
0	0	0	1	1	1
0	1	1	0	1	1
1	0	0	0	0	1
1	1	0	0	1	0

TABLE I (B): TRUTH TABLE OF COLUMN DECODER



(a) Schematic of odd row of local decoder and varactor cell in varactor array.

R_N	R_{N+1}	C	Varactor cells in R_N and R_{N+1} rows are
0	0	X	ON
0	1	0	OFF
0	1	1	ON and OFF respectively
1	0	0	ON
1	0	1	ON and OFF , respectively
1	1	X	OFF

Please note, that switched ON and OFF means is that output capacitance of varactor cell is LOW and HIGH, respectively. Here again we defined the three state of row ON, ACTIVE, OFF. Row # ON, OFF and ACTIVE signifies that all varactors in row # are ON, OFF and status depends on column signal. For odd and even row of status ACTIVE varactor cell will be ON if column signal is high or low, respectively.

The main advantages of this scheme is that

1. It reduces the number of signal lines to 32 for 16 by 16 matrix as compared to 48 in [4].
2. Conventional decoder can be implemented by 32 lines, but every line needs to be vertically routed for 16 local decoder to the adjacent row which is equivalent to 48. Also, additional space is required to isolate these lines with column and RF signal lines. But in proposed logic no row line need not to be vertically routed.

INPUT signal			OUTPUT signal			
D2	D1	D0	C1	C2	C3	C4
0	0	0	1	0	0	0
0	0	1	1	1	0	0
0	1	0	1	1	1	0
0	1	1	1	1	1	1
1	0	0	1	1	1	0
1	0	1	1	1	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0

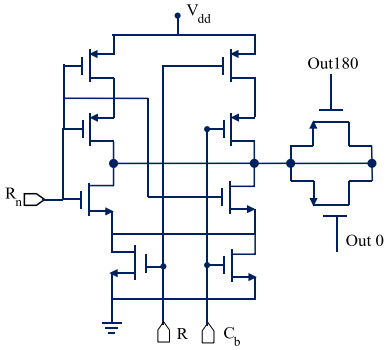


Fig.3. Layout of varactor array for 2 bit by 2 bit.

3.3 Layout Consideration

The proposed decoder require only 32 digital signal interconnect lines as compare to 48 in [4]. These signal lines runs parallel in layout so they must have some minimum distance to reduce the parasitic capacitance and to avoid switching disturbances. This space should be further increased if digital signal lines run parallel with RF signal lines. In [4] 32 digital signal lines with 16 RF lines runs in 16 rows. This means in each row two signal andone RF line. To isolate RF signal line with digital signal at least 2 times space is required so for 16 lines this comes to be 32 which is significant. In our layout, digital and RF signal lines run in separate rows and separated by digital blocks. Digital signal lines run in odd row and RF signal in even rows.

In Fig. 6. layout is demonstrated for 4 control bits. Higher order 2 bit are converted into 4 digital signal (R1-R4) and lower order 2 bits into 4 digital signal (C1-C4) by row and column decoder, respectively as per the proposed logic.Rf1 and Rf2 are varactor output lines. The layout is made to reduce the area and parasitics.

4. SIMULATION RESULT OF DCO

The DCO was designed in 0.18 µm CMOS technology to test the proposed optimization technique for DNL, capacitive mismatch and tuning range. The proposed DCO layout is designed using cadence layout tools.

Fig. 7 shows the simulated tuning range of the DCO. Tuning range is measured by fixing CTW and varying FTW from 0 to 1023. Fine tuning code is plotted on X-axis. The tuning curve shows four lines for CTW00, 01, 10 and 11. The DCO operates between 3.12–3.38 GHz at CTW= $(00)_2$, 3.31–3.59 GHz at CTW= $(01)_2$, 3.52-3.85 GHz at CTW= $(10)_2$, and 3.78- 4.15 GHz at CTW= $(11)_2$ and the simulated data curves show highly monotonic behavior.

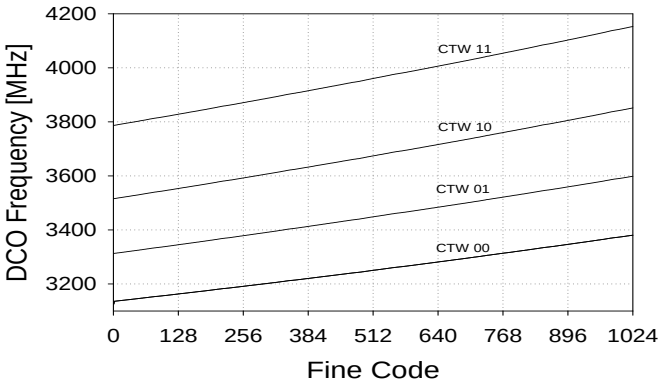


Fig.4.Simulated tuning range for CTW= $(00)_2$, CTW $(01)_2$, CTW $(10)_2$ and CTW $(11)_2$.

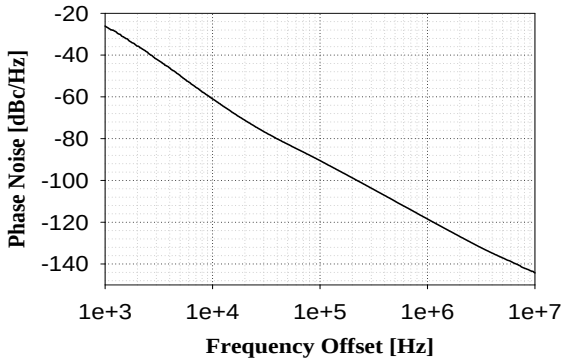


Fig.5. Simulated phase noise of proposed DCO. f_{osc}=3.8 GHz, CTW= $(11)_2$.

The simulated phase noise spectrum is shown in Fig. 8 where the phase noise is -135.2 dBc/Hz at 4 MHz offset from the center frequency of 3.8 GHz.

Fig. 9 shows the DNL for the 10 bits FTW. The measured DNL is -0.41 LSB which is less than 0.52 LSB reported in [4] which shows that proposed optimization technique is not followed. The measured DNL is not high, rather it is as expected since DNL have contribution of -0.13 LSB and -0.15 LSB due to nonlinear mathematical equation and mismatch among varactor cells and rest of the values is added due to various gradient. The power dissipation of the proposed oscillator is 19.8 mW.

TABLE II
DCO PERFORMANCES COMPARISON

DCO	Tech. [nm]	TR [%]	DNL [LSB]	Phase Noise [dBc/Hz]	Power [mw]	FOM [dBc/Hz]
[3]	130	20%	-	-112@ 0.5MHz	3.5	-180.1
[4]	65	10%	0.52	-102@ 1MHz	3.3	-176.9
[5]	130	26%	-	-118@ 1MHz	8.0	-175.0
This	180	30%	0.41	-135.2 @4MHz	19.2	-182

DCO	CTB	CTS [MHz]	FTB [LSB]	FTS [kHz]	DCO Size [mm^2]
[3]	8	2.316	8	461	0.54
[4]	-	-	10	1030	0.026
[5]	10	1	10	200	0.19
This	2	300	10	360	0.24

In Table II, the overall performances of the proposed DCO is compared with other published DCOs where figure of merit (FOM) is comparable or slightly better than other DCOs but the main advantage of this DCO is the good linearity and highly monotonic behavior compared to others. A widely-

known equation (11) [11] is used to compute figure of merit (FOM) of the DCO and compared the results in Table II.

$$FOM = L\{\Delta f\} - 20\log\left\{\frac{f_0}{\Delta f}\right\} + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (11)$$

Here, $L\{\Delta f\}$ is the measured phase noise at offset frequency $\{\Delta f\}$ from the carrier frequency f_0. P_{DC} is VCO power consumption in mW. The measured FOM is –182dBc/Hz at 3.8 GHz frequency

5. Conclusion

A 12 bits DCO is designed employing the proposed mathematical model for optimization of DNL and tuning range for a given frequency tuning step. DNL is within the limits and highly monotonic frequency tuning curve is achieved with 12 bits digital control codes. Varactor array is implemented is implemented using new decoding scheme which reduces the area about 40% proposed which significantly reduces the parasitic. The tuning range of the proposed DCO is very close to 30% which is the theoretical limit of a LC-oscillator without using any frequency tuning extension circuits under the design limit of DNL. This monotonic behavior of the DCO will ease the design of an all-digital phase locked loop for wireless transceiver, which will be taken as one of the most important future works.

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