KIET IJCE KIET International Journal of Communications & Electronics
Volume. No. 2, Issue No. 1, Jan –April 2014, ISSN: 2320 - 8996

Design and implementation of Phase Frequency Detector Using Different Logic Gates in 45nm CMOS Process Technology

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***Abstract*— The Phase Detectors determines the relative phase difference between the two incoming signals and outputs a signal that is proportional to this phase difference. The phase detector also detects the frequency error; they are called Phase Frequency Detectors (PFD). It is very important block for the PLL Frequency synthesizer. This paper presents the different design schemes of the PFD and compares them with their output results. The PFD is implemented with True Single Phase Clocked logic. The circuits that have been considered are the PFD using NAND Gate, PFD using NOR Gate and PFD using AND Gate. The different PFD circuits are designed and simulated on Tanner EDA Tool using 45nm CMOS process technology with supply voltage 1 V.**

Keywords- **Phase Frequency Detector, Phase locked loop, True Single Phase Clocked, Tanner Tool.**

I. INTRODUCTION

The rapid growth in wireless applications in last decade has motivated to design fully integrated, low power, low cost and high performance transceivers. Most of the wireless implements frequency using PLL Frequency Synthesizer. PLL Frequency Synthesizer finds wide application in areas such as communication, clock generation circuits [1], wireless systems, digital circuits. The basic building block of PLL Frequency Synthesizer consist of phase frequency detector (PFD), loop filters, charge pump, voltage control oscillator (VCO) and programmable frequency divider as shown in fig.1.

PFD in PLL is used to detect the phase as well as frequency difference between the two signals that is reference signal and the output from VCO as compare to the phase detectors which are capable of detecting the phase difference only. The characteristics of PFD have huge impact on performance of PLL. The lock time and timing jitter of a PLL are largely affected by the characteristics of phase frequency detector

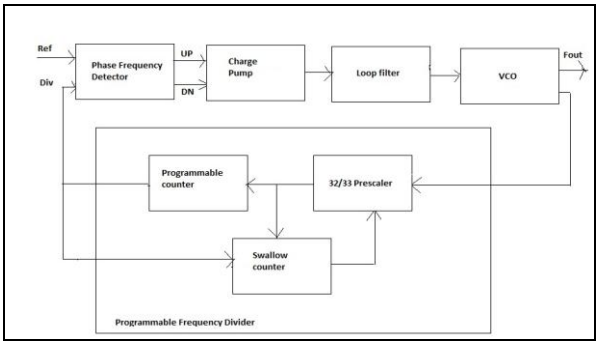

Fig.1 Block diagram of PLL Frequency Synthesizer

II. DESIGN ISSUES

The main two design issues which should be taken into account are dead zone and blind zone. If the phase difference between the clocks at the input of the phase detector is smaller than a certain value, then the control voltage is not a function of the phase difference. This is basic definition of dead zone. Dead zone is due to the delay time of the logic components of digital circuit and the reset time that requires by the reset path to reset the flip flops of the PFD [2].

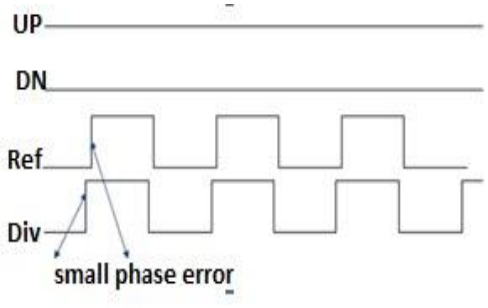

Fig. 2 Dead Zone

III. CIRCUITS ARCHITECTURE

A. NAND gate based PFD

The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a NAND Gate in the reset path [3]. The explanation of the general operation of the PFD begins by describing the initial state of the device. First, the UP and DN signals are reset to low or zero and assume both the Ref frequency signal and the Div signal are high or one. Additionally, the Ref frequency waveform is slightly leading the Div waveform. When a falling edge occurs on the Ref input, the high or one on the D input is transmitted to the Q output or UP. A short time later, the Div waveform experiences a falling edge and the Q output or DN of the other flip flop is set. Once both UP and DN are high or ONE, the NAND gate experiences a transition to force the Reset signal to zero. The flip flops are designed so that zeros on the Reset signal resets the Q outputs to zero.

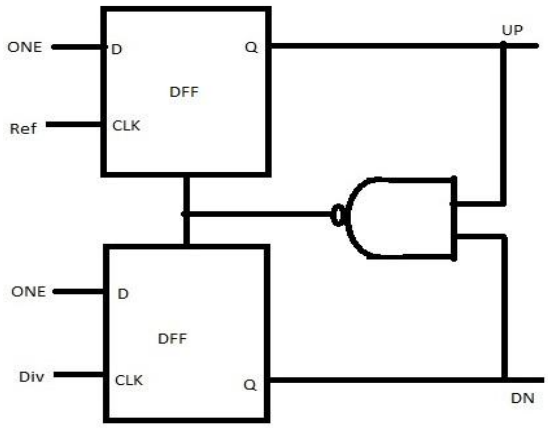

Fig.3 NAND Gate based PF

The PFD is implemented with True Single Phase Clocked logic. The design strategy is to minimize the number of transistors and the amount of power consumed. However, not all of the transistors can be implemented with minimum width such as those involved in the reset operation. The schematic of PFD using NAND Gate is shown in Fig.4.

B. NOR gate based PFD

PFD using NOR gate is shown in figure.5. The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a NOR Gate in the reset path [6]. The Ref and Div serve as clocks of the flip flops. The UPb and DNb signals are given as input to the NOR gate. Suppose the rising edge of Ref leads that of Div, then UPb goes to logic low i.e. UP keeps high until the rising edge of Div makes DNb on low level. Because UPb and DNb are NORed, so Reset goes to logic high and resets the PFD into the initial state.

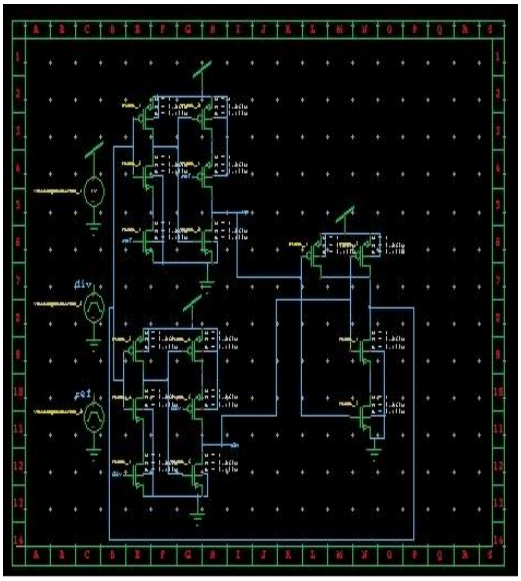

Fig.4 Schematic of NAND Gate based PFD

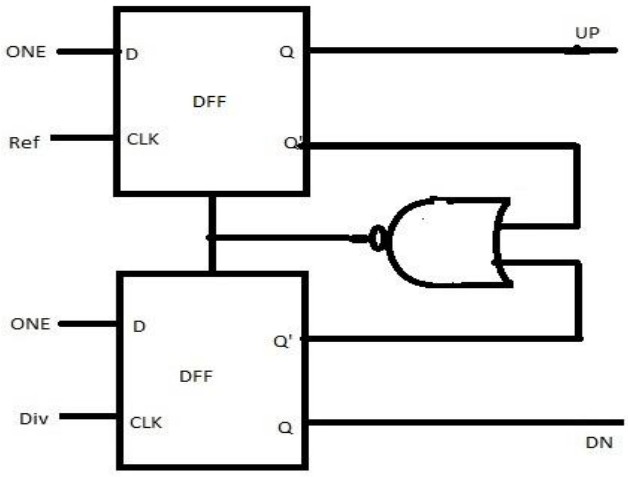

Fig.5 NOR Gate based PFD

The schematic of NOR Gate based PFD shown in Fig.6 which consisting of only 20 transistors.

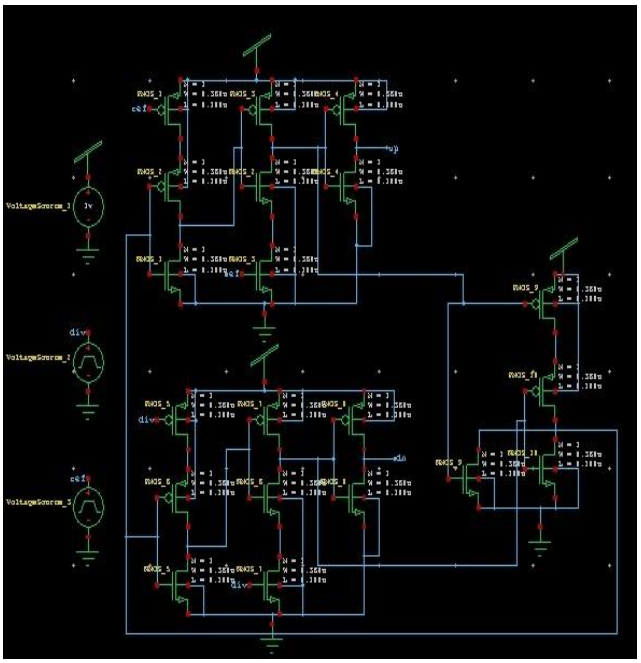

Fig.6 Schematic of NOR Gate based PFD

C. AND gate based PFD

Fig.7 shows the PFD using NOR gate. The circuit consists of two edge triggered D flip flops DFF which is resettable, with their D inputs tied to logic 1 and a AND Gate in the reset path [7]. The Ref and Div serve as clocks of the flip flops. Suppose the rising edge of Ref leads that of Div, then UP goes to logic high. UP keeps high until a low to high transition occurs on Div. Because UP and DN, are AND, so Reset goes to logic high and resets the PFD into the initial state.

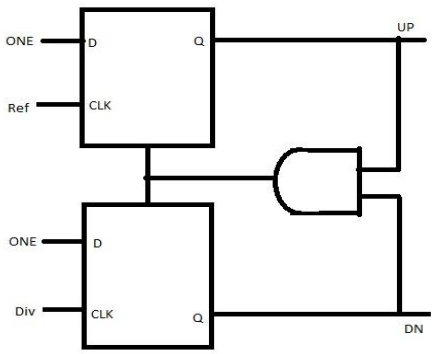

Fig.7 AND Gate based PFD

The schematic of AND gate based PFD circuit consisting of only 22 transistors is shown in Fig.8

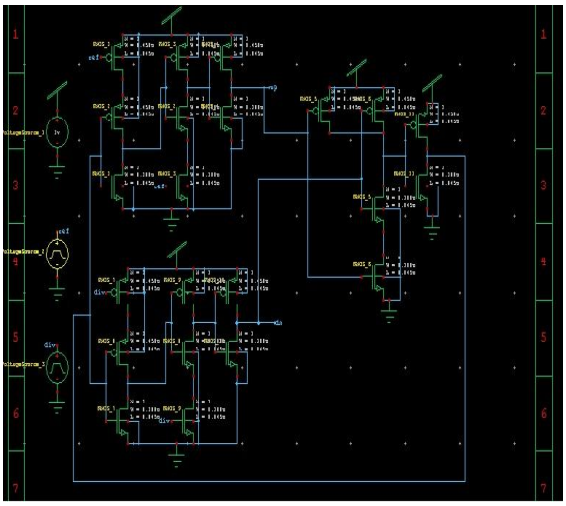

Fig.8 Schematic of AND Gate based PFD

IV. SIMULATION RESULTS

The PFD is a state machine with three states. When Ref leads Div, the UP output is asserted on the rising edge of Ref. The UP signal remains in this state until a low to high transition occurs on Div. At that time, the DN output is asserted causing both the flip flops to reset through the asynchronous reset signal. There is a small pulse on the DN output, whose duration is equal to the delay through the logic gates and the reset delay. The pulse width of the up pulse is equal to the phase error between the two signals.

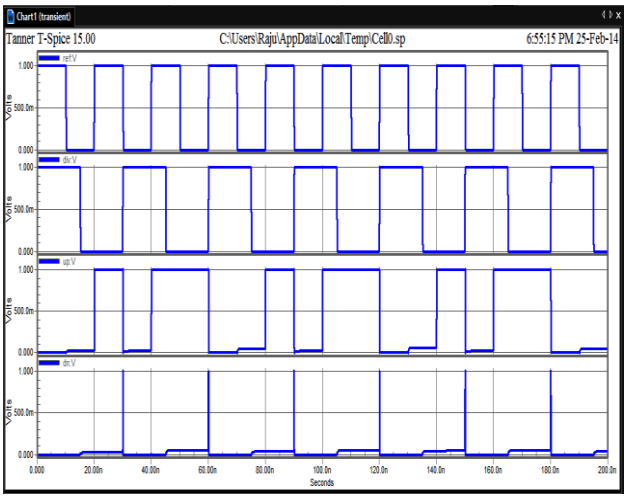

Fig.9 AND Gate PFD simulation I(Ref signal leads Div signal)

In the second case, ref signal is lagging Div signal. In this DN pulse represents the difference between the phases of two clock signals.

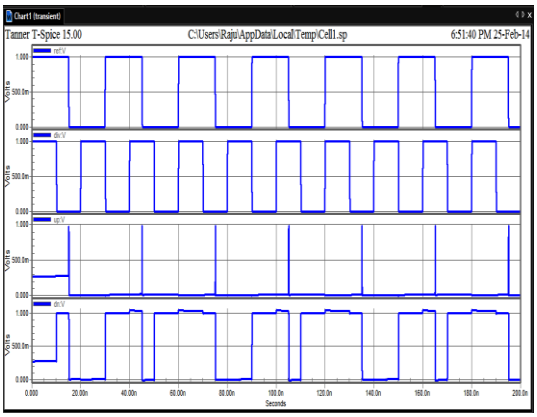

Fig.10 NOR Gate PFD simulation II (Div leads Ref signal)

In the third case, Ref signal is in phase with Div signal, which is shown in Fig. 10. In this case, the loop is in locked state and short pulses will be generated on the up and DN outputs.

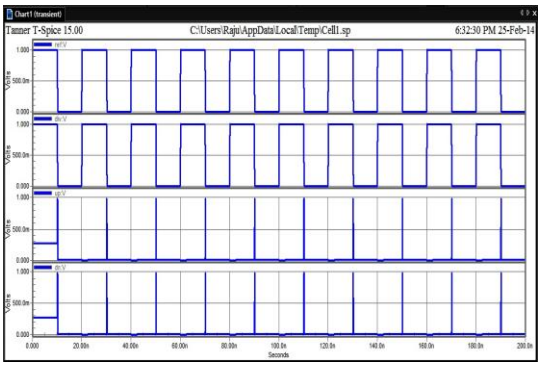

Fig.10NAND Gate PFD simulation III (DIV is in phase with Ref signal)

V. PERFORMANCE COMPARISON

Table I represents various parameters for the different PFDs when they are designed on Tanner 15.0v. It is seen that NAND based PFD has the minimum power consumption and occupy less area compared to the other two. They all have the same range of operating frequency. Dead Zone problem is also negligible for the NAND Based PFD.

Table I: Comparison between different PFD

Parameters	**AND Based PFD**	**NOR Based PFD**	**NAND Based PFD**
Operating Frequency	1 GHz	1 GHz	1 GHz
Glitch Period	5.18ns to 5.75ns	5.14ns to 5.68ns	5.18ns to 5.43ns
Glitch Time	657ps	547ps	375ps
Delay	2.4525e-008 sec	4.6767e-009 sec	5.6797e-005 sec
Transistor Counts	22	20	16
Dead Zone	50ps	40ps	25ps
Power Consumption	2.148780 e-005W	2.58299 e-005W	2.912447 e-005W

VI. CONCLUSION

Minimization of power consumption is essential for high performance VLSI systems. This paper compares the performance of Phase Frequency Detectors by different Logic Gates .As can be seen from the simulation results AND based PFD consumes maximum amount of power among all the PFDs and has highest delay. NOR based PFD consumes more area and power compared to the NAND based PFD. Therefore, in order to have low power consumption and smaller area we use NAND based PFD which is also having approximately zero Dead Zone problem.

ACKNOWLEDGEMENTS

I am thankful to my parents, my special friends to motivate me and to increase my confidence. I am thankful to B.H.Narpara Khandhar sir and B.H.Narpara sir to guide me. And finally I am thankful to hidden energy to stay always with me.

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