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Cost Comparison Parameters for Quantum-Dot Cellular Automata Designs

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***Abstract*— Quantum-dot cellular automata (QCA) technology has become an alternative to CMOS technology for future digital designs because it give low power dissipation, high density and no leakage current compared to CMOS Designs. Many circuits are studied in QCA technology. But how to examine that which QCA Design is better than any other QCA design is not considered yet. Until now, parameters and area-delay cost functions are directly used from CMOS technology to compare QCA designs. This is not an appropriate approach because both the technologies are different. Therefore in this paper, several cost parameters are proposed which helps in evaluation of QCA Designs. And through these parameters it is found that the number of QCA logic gates, the delay and the number and type of crossovers, are the main parameters which effect QCA designs and must be considered before choosing any design for an application.**

***Keywords*— Quantum-dot cellular automata (QCA), cost functions, parameters.**

I. INTRODUCTION

Quantum-dot cellular automata (QCA) [1] technology have become possible replacement to CMOS technology. QCA provides various advantages like fast speed, low power consumption and high density, which have the capability to maintain the trend of Moore's Law. Many novel approaches are offered by QCA in computation and communication which are "processing-in-wire" and "memory-in-motion" [2] and so it is used as an nanoscale technology for the development of digital systems.

Until now, the circuits having only local interaction in QCA have been implemented Designs. In this interaction both electrostatic interaction (molecular, semiconductor, and atomic) and magnetic interaction QCAs have been implemented and investigated. At present semiconductor QCA can only work at low temperatures. However, as the technology is developing, the temperature range may vary. Arithmetic circuits, memory, and simple processors have been designed and analyzed with QCA Designer [2]. But the manner in which to compare and analyze QCA designs are not studied.

As addition is considered as the heart of computer arithmetic calculation, and a designer would like to make the best adder in their designs, but what defines the "best" adder in QCA technology? In previous research it was found that multilayer QCA circuits are preferred over the coplanar circuits because they offer better area, latency, and the number of cells [3], which are directly used from CMOS parameters. But the difference between both the multilayer crossovers and coplanar crossovers is not considered and there are no parameters provided for their comparison. Multilayer crossovers consume less area compared to coplanar crossovers and the cost of fabrication of multilayer crossovers is more compared to that of coplanar crossovers. As CMOS and QCA technologies are both different so previous parameters and area-delay cost functions can't be used for true comparison. So, new parameters and specific cost functions for the QCA circuits need to be investigated that can help in guiding the optimization of the QCA circuit designs.

In this paper, the evolution of the cost parameters of CMOS technology is considered so that the ideas are generated for the cost parameters of QCA Designs. Based on this analysis of all present parameters, a group of new QCA cost functions is proposed. The proposed cost functions can be used to examining the performance of any QCA circuit. Adder designs are selected in QCA Designs because adder designs are the heart of the computer calculations. Than in future QCA adders are compared based on these parameters and then examined with both the CMOS area-delay cost function and proposed QCA cost functions in terms of the overall cost. And final comparison results show that the selection of the "best" adder is based on the design of application and also differs between technologies. This paper is a first step to evaluate the overall cost of QCA circuit design and it is anticipated that further consideration of cost functions for QCA designs will be inspired by this paper.

The remainder of the paper is organized as follows. Section II presents the QCA basics. In Section III, several comparison parameters are studied. Section IV provides the proposed QCA cost functions. Conclusions are given in Section V.

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II. QCA BASICS

A. QCA Cell

A basic QCA cell that is made of four quantum dots which can bind electron within it is shown in Fig. 1(a). All the dots are connected with each other via a tunneling wire through so that electron can tunnel among all four dots. First two extra free electrons are added within QCA cell and as the electron repulsive force between them are placed at antipodal position within QCA cell. Depending on this position of electrons two different structures of QCA cell may exist, called polarization of the QCA cell and denoted. P=+1 and P=-1 indicates the binary logic values '1'and '0'respectively and P=0 specifies an un-polarized cell in Fig. 1(b) i.e., contains no information. The rotated cells are used for coplanar crossings as shown in Fig. 2.

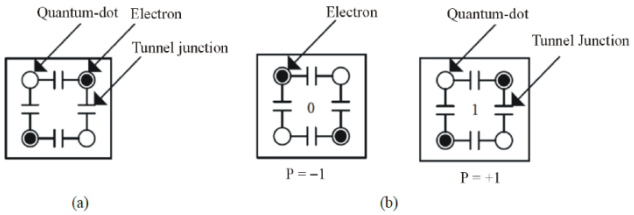

Fig 1. QCA Regular cell polarization

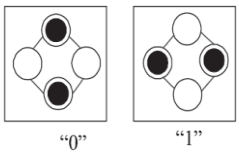

Fig 2. QCA Rotated Cell

B. QCA Wire and Logic Gates

In contrast to a physical wire, a QCA "wire" is a chain of cells where the cells are placed adjacent to each other as shown in Fig. 3. The QCA logic gates are three-input majority gates and inverters. An inverter is designed by diagonally placing cells from each other and different structures are also present as shown in Fig. 4(b). Inverters can usually be included in the interconnections and do not provide any additional delay. A three-input majority gate consists of five QCA cells which have the function of $M(a, b, c) = a\,b + b\,c + a\,c$ as shown in Fig. 4(a). A 2-input OR gate or a 2-input AND gate can be implemented by fixing one of the majority gate inputs to "1" or "0", respectively. In combination with inverters, these two logic components can be used for implementation of logic function.

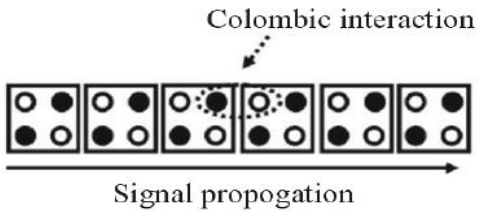

Fig 3. QCA Wire

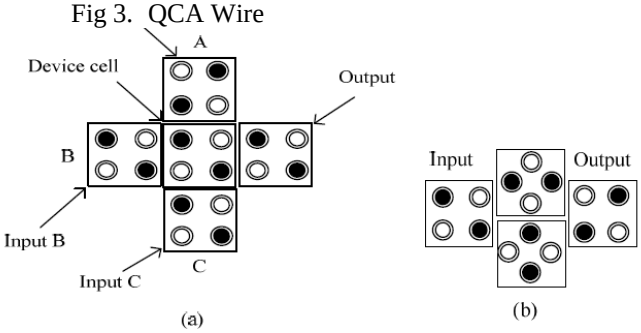

Fig 4. QCA (a) Majority Gate and, (b) Inverter

C. QCA Wire and Logic Gates

QCA clocking is made of four phase shift by 90^o as shown in fig.4 which creates a new path to design nano-circuits. The clock signals of QCA circuits are generated by an electric field which is applied to the QCA cells to modulate the tunneling barrier between dots (i.e., inter dot barrier). The physical raising and lowering of the barriers depends on the actual phase of technology. Four phases of clock are as follows:

Switch phase— the barrier between dots of QCA cell is increased. The quantum dots are influenced by the electron of its neighboring and electron starts tunneling between dots. So the QCA cell becomes in polarized state.

Hold phase— barrier of the cell remains high and electron can't tunnel between dots and the cell maintains its current states (fixed polarization).

Release phase— barrier between dots are decreased, electron can tunnel through dots and QCA cell become in un-polarized state.

Relax phase— barrier stay at lowered and cell remains in un-polarized state.

The smallest unit of delay in QCA is a clocking zone delay that is quarter of a clock cycle.

Two types of clocking floorplans can be used in QCA circuit implementations, namely columnar regions and zone regions as shown in Fig. 5. The columnar approach is considered to be more practical for physical implementation than that of zone approach. However, it has difficulty in realizing high circuit densities and short feedback loops. On the other hand, the zone approach can achieve all this. Smaller zones are more difficult to implement, but are considered as

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more area efficient. Using large clocking zones reduces the clock speed for reliable operation and increases the delay of the circuit.

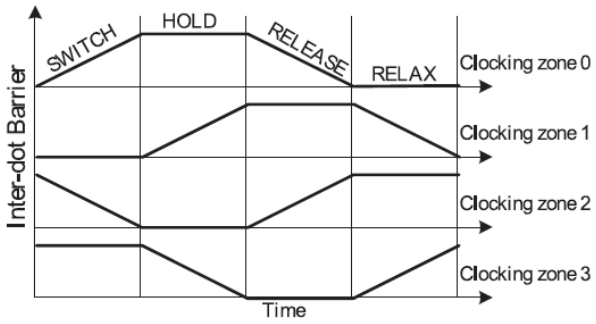

Fig 5. QCA clocking Scheme

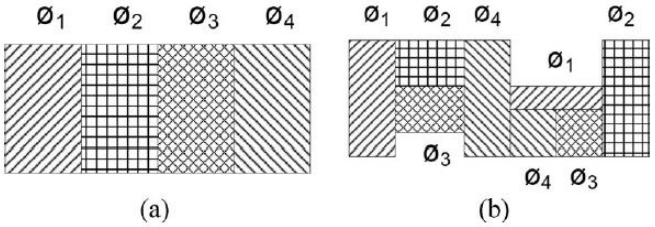

Fig 6. QCA clocking floorplans: (a) columnar Region and (b) zone Region.

Therefore, there is a tradeoff between the size of clocking zones and the circuit stability and efficiency. For semiconductor QCA, it is possible to clock QCA cells individually. As a result, small zones can be used for clocking. However, for magnetic and molecular QCA, columnar clocking zones are generally used. This study is based on semiconductor QCA. Therefore, small zones are used for the QCA designs.

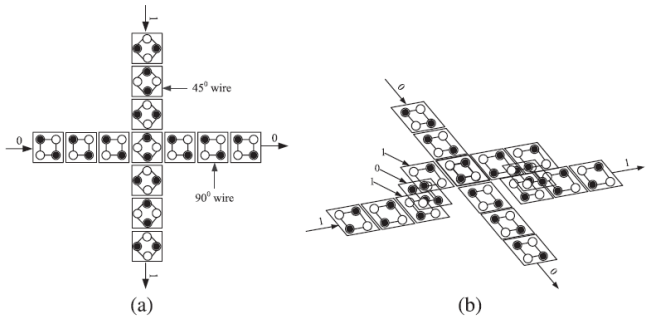

Fig 7. Crossovers in QCA: (a) Coplanar crossovers and, (b) Multilayer crossovers.

D. QCA Wire Crossings

In semiconductor QCA technology, two wire crossing options are available, that are multilayer crossovers and coplanar crossings. A coplanar crossing was proposed [4] as a unique property of a QCA layout which implements the crossovers by using only one layer, as shown in Fig. 7(a). A coplanar crossing can use both regular and rotated cells that do not interact with each other when they are properly aligned. The other alternative is multilayer crossing , which uses more than one layer of cells as shown in Fig. 8(b). However, multilayer crossovers are not easy to fabricate due to the structure of multiple layer. The cost of fabricating a multilayer crossover is expected to be significantly greater than that of a coplanar crossing because of difficulty to fabricate it.

III. COST PARAMETERS

Area, delay, and power consumption are considered as the main parameters for CMOS circuits and on the basis of these parameters the quality of CMOS circuits are measured. In the past, the main concern of a CMOS circuit was as the area of circuits because it was directly related to the cost of the design. But as the feature size is decreased very much due to the advancement in the fabrication technology and now area is not the major concern and the main goal has changed to the speed and performance of the device. Thompson has proposed various models of the area-time [7] and he proposed the CMOS cost function as:

$$\text{Cost Area–Delay} = A \times T^n \ , 0 \leqslant n \leqslant 2 \qquad (1)$$

Where A is the area and T is the delay of a CMOS circuit. Based on Mead and Rem's VLSI model theory of bisection problem Lower bounds of cost functions were derived [9]. For a QCA also a minimum unit of time is needed to transmit information in QCA wires, which is a clocking zone delay (equal to a quarter of a clock cycle) . This suggests that the models of (1) may also be applicable to QCA technology. Transistor size can improve the speed of a circuit while at the same time it increases the power dissipation. Therefore, cost functions that involve power delay are as follows :

$$\text{Cost Power–Delay} = P^m \times T^n \qquad (2)$$

Where P is the power dissipation and it is determined by dynamic power dissipation in CMOS technology. The dynamic power dissipation is given as:

$$P_{\text{Dynamic}} = \alpha \, C_L \, (V_{dd})^2 f \qquad (3)$$

Where α is the activity factor, C_L is the load capacitance, V_{dd} is the supply voltage, and f is the clock frequency. As irreversible power dissipation from bit erasures (which is negligible in CMOS) dominates the total power dissipation in QCA, the power dissipation issue is different from that of

CMOS must also be considered. Similar to CMOS, the cost metrics for QCA circuits need to be carefully investigated as these can significantly affect the choice of QCA designs. In this section, some new metrics including the number of logic gates, the irreversible power dissipation, and the number of crossovers are investigated.

A. Delay

Delay is considered as an vital parameter for assessing the performance of circuits. Various circuits are applied with the same clock rate, so the number of clocking zones present in the circuit is considered as the measure of the latency i.e Delay. And it is determined as the number of clocking zones times the clock period along its path of information flow and better QCA circuit designs use fewer clocking zones. Therefore, the delay of a QCA circuits should also be included in a cost function. The minimum delay in QCA is a clocking zone delay and it is 1/4 of a clock cycle.

B. Area/Complexity

The number of cells in QCA circuits is similar to the number of transistors in CMOS circuits. In a QCA circuit logic components and connecting wires are both combination of QCA cells. Therefore, the number of cells in a QCA circuit is considered to be directly proportional to its area and including both the logic components and the QCA wires would result in a double weighted area parameter [4]. So, any one of them can be used to measure the complexity of a QCA circuit. The area of QCA designs is mainly dependent on types of crossovers present in the circuit. Therefore, if only area is considered for comparison of QCA Designs it will lead to wrong result. Therefore to measure the complexity of a QCA circuit, the numbers of logic gates and crossovers are best parameters. Therefore, the circuit complexity in QCA is actually the sum of the three elements: majority gates, inverters and crossovers.

C. Irreversible Power Dissipation

In integrated circuits the major limiting factors is the power dissipation. Even the power dissipation in QCA designs is very small, but QCA circuits have thermal problems due to high density. Bit erasures generate "irreversible dissipation" which is negligible in the traditional technology, it becomes a major limitation in computers with ultrahigh density at nanoscale integration. It has been proved experimentally that the power dissipated in the clocking wires is small [4].

QCA "wires", are combination of QCA cells, and each cell can be considered as shift registers which stores the values and which have one input and one output and due to this it is reversible cell and therefore it dissipates little power [5]. Similarly, the inverter gate is also a logically reversible unit, which consumes less power. The irreversible dissipation mostly occur in the three-input majority gate, because it have three input but only one output so there is no balancing between input and output and due to this there is significant information loss and unavoidable power dissipation, which is equivalent to the activity factor (α). Different algorithms and architectures use different numbers of majority gates, which leads to different activity factors. Therefore, majority logic reduction methods should be employed in QCA designs so that less cost efficient design is obtained [5].

D. Number of Crossovers

Crossover refers to the two separate signal wires in the circuit at the same point and it also very important parameter in QCA technology. The coplanar crossings use only one layer, but require careful alignment of cells during fabrication and the other crossing is the multilayer crossover. Gin etal discovered the original idea of multilayer QCA circuits, which is applied to multilayer crossovers in many QCA designs.

For a multilayer crossover, minimum of three layers are required to implement the crossings and the distance between two vertical neighboring layers needs to be arranged properly so that the kink energy is matched to that of normally adjacent cells, which is difficult to obtain. As a result, complexity increases in fabrication of multilayer crossovers compared with coplanar crossings.

To do clocking in both crossover types is very difficult during operation. For coplanar crossings, very fine clocking zones are required for signal propagation. The clocking of multilayer crossovers is also very difficult. Thus, when more crossovers are used in a QCA circuit, it becomes more difficult to fabricate the circuit [10].

And the cost of a multilayer crossover is greater than that of a coplanar crossing, which suggests a cost model as follows:

$$C_{ml} = m \times C_{cp} \qquad (4)$$

Where, C_{ml} is the cost of a multilayer crossover, C_{cp} is the cost of a coplanar crossing, and m is a coefficient to reflect the higher cost of a multilayer crossover to coplanar crossing. If a multilayer crossover uses at least three single layers, m is assumed to be 3 or more. Minimizing the number of crossovers is always desirable in QCA circuit design [10]. Thus, the number of crossovers is very important parameter in QCA that must be included in QCA cost functions.

IV. Proposed QCA Cost Parameters

Based on the above cost parameters either the number of cells or the area can be used as the cost function for comparison of the designs. So to measure the complexity of a

QCA circuit, the numbers of logic gates and crossovers are considered as the parameters. The majority gates have irreversible power dissipation and crossovers are associated with fabrication difficulty. Therefore, they should have higher weightings. Delay is always important due to the performance considerations. For these reasons, the delay, number of logic gates, and number of crossovers are used as a measure of the performance, complexity, irreversible power dissipation, and the fabrication difficulty of a QCA circuit. A generalized QCA cost function is as follows:

$$\text{Cost QCA} = (M^k + I + C^l) \times T^p, 1 \leqslant k, l, p \qquad (5)$$

Where, M is the number of majority gates, I is the number of inverters, C is the number of crossovers, T is the delay of the circuit, and k, l, p are the exponential weightings for majority gate count, crossover count and delay, respectively. A constant weighting of *"1"* is assigned to the number of inverters, as inverters only affect the complexity of QCA circuits. These cost functions are similar to the CMOS area-delay cost functions as in (1). The cost functions prioritize different parameters according to the weightings k, l, and p. For example, if speed is a primary concern, more weight can be given to the delay parameter, i.e., a higher value of p. If fabrication cost is more important, the value of l should be higher than that of p and k and so on. Therefore, the weight values can be adjusted depending on the overall design optimization goal.

V. Conclusions

Many cost related parameters are specified in QCA circuits which must be considered while comparing the QCA designs. Based on the above analysis, the delay, the number of majority gates, and the number of crossovers are the important parameters of a QCA design can be used as cost function for circuits. A family of cost functions was proposed, Cost = $(M^k + I + C^l) \times T^p$, for the comparison of QCA circuits. Based on these cost functions the performance, complexity, irreversible power dissipation, and the fabrication difficulty of a QCA circuit can be measured. And this can be used as the basis for telling which QCA Designs are optimized according to need of the application.

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